AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A data processing circuit having a nonvolatile memory and a central processing circuit structured on one semiconductor substrate,

wherein said nonvolatile memory is capable of storing a program and/or date,

wherein said central processing circuit is capable of fetching said program from said nonvolatile memory,

wherein said nonvolatile memory comprises bit lines, word lines, and memory cells,

wherein said memory cell comprises a MOS transistor whose gate electrode is connected with a word line, and information storage is carried out according to whether one source/drain electrode of said MOS transistor is connected with a current path or floated, and

wherein a control circuit is provided which produces a potential difference between the source/drain electrodes of said MOS transistor during a predetermined period in the operation of accessing said memory cell, and makes zero the potential difference between the source/drain electrodes of said MOS transistor during periods other than said predetermined period.

2. (Previously Presented) The data processing circuit according to Claim 1, wherein the time at which a potential difference is produced between the source/drain electrodes of said MOS transistor is matched with or behind the time at which a word line is selected.

3. (Previously Presented) The data processing circuit according to Claim 1, wherein said nonvolatile memory and said central processing circuit use a common supply voltage as their operating power supply voltage.

4. (Previously Presented) The data processing circuit according to Claim 1, wherein whether a MOS transistor is connected with said current path or floated is determined according to whether the one source/drain electrode thereof on an opposite side to the bit line is connected with a predetermined signal line or not.

5. (Previously Presented) The data processing circuit according to Claim 1 or Claim 4, wherein the MOS transistors respectively included in a plurality of memory cells disposed along said bit lines are formed in a common well, and are electrically separated from each other by a dummy MOS transistor whose gate electrode is supplied with an off potential.

6. (Previously Presented) The data processing circuit according to Claim 4, wherein one memory cell has two MOS transistors, and the other source/drain electrodes of the two MOS transistors are connected with separate bit lines which comprise complementary bit lines and the gate electrodes of the two MOS transistors are connected with a common word line.

7. (Previously Presented) The data processing circuit according to Claim 5, wherein one memory cell has two MOS transistors, and the other source/drain electrodes of the two MOS transistors are connected with separate bit lines which comprise complementary bit lines and the gate electrodes of the two MOS transistors are connected with a common word line.

8. (Previously Presented) The data processing circuit according to Claim 6, further comprising an amplifier which amplifies the potential difference between said complementary bit lines.

9. (Previously Presented) The data processing circuit according to Claim 7, further comprising an amplifier which amplifies the potential difference between said complementary bit lines.

Claims 10-11. (Canceled without prejudice or disclaimer).

12. (Previously Presented) A data processing circuit having a nonvolatile memory and a central processing circuit structured on one semiconductor substrate,

wherein said nonvolatile memory is capable of storing a program and/or data, and comprises memory cells, word lines, complementary bit lines, and differential amplifiers connected with said complementary bit lines,

wherein said central processing circuit is capable of fetching said program from said nonvolatile memory,

wherein said memory cell comprises a pair of MOS transistors whose gate electrodes are connected with the same word line; one source/drain electrode of each of said pair of MOS transistors is separately connected with a corresponding bit line of the pair of complementary bit lines, the other source/drain electrode of one of said pair of MOS transistors is connected with a voltage signal line supplied with predetermined voltage, and the other source/drain electrodes of the other of said pair of MOS transistors is floated

wherein said memory cell is capable of storing data in accordance with said voltage signal line being connected with the other source/drain electrode of said one of said pair of MOS transistors, and

wherein during a predetermined period in the operation of accessing said memory cell, voltage is applied to said voltage signal line which voltage produces a potential difference between the voltage signal line and said bit line, and during the other periods than said predetermined period, voltage is applied which makes zero the potential difference between the voltage signal line and said bit line.

13. (Previously Presented) The data processing circuit according to Claim 12, wherein said nonvolatile memory and central processing circuit use common supply voltage as their operating power supply voltage.

14. (Previously Presented) The data processing circuit according to Claim 12, wherein during the other periods than said predetermined period in accessing operation, said voltage signal lines and complementary bit lines are brought to supply voltage, and during said predetermined period, said voltage signal lines are discharged to the ground voltage of the circuit.

15. (Previously Presented) The data processing circuit according to Claim 14, wherein the time at which said voltage signal lines are discharged to the ground voltage of the circuit during said predetermined period is matched with or behind the time at which a memory cell is selected by word line.

Claims 16-31 (Canceled without prejudice or disclaimer)